| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/466,665 | MOSER ET AL. | |
| | Examiner | Art Unit | |
| | Curtis B. Odom | 2634 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdt filed on 7/16/04*.

2. ☒ The allowed claim(s) is/are *1-32, 35, 36, 38-68, and 70-78, which have been renumbered claims 1-74, respectively*.

3. ☒ The drawings filed on *20 December 1999* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Kent Daniels on October 4, 2004.

The application has been amended as follows:

Claim 4 (currently amended) A digital frequency detector as claimed in claim 1, wherein the first sample means comprises:

a) a pair of digital latch circuits respectively adapted to sample the oscillator output signal on rising and falling edges of the data signal; and

b) a multiplexor adapted to selectively switch between respective outputs of the pair of digital latch circuits on transitions of the data signal.

Claim 5 (currently amended) A digital frequency detector as claimed in claim 1, wherein the second sample means comprises:

a) a pair of digital latch circuits respectively adapted to sample the quadrature clock signal on rising and falling edges of the data signal; and

b) a multiplexor adapted to selectively switch between respective outputs of the pair of digital latch circuits on transitions of the data signal.

Claim 14 (currently amended) A digital frequency detector as claimed in claim 13, wherein the third beat signal is generated by a multiplexor adapted to alternately select respective outputs of a pair of digital flip-flop circuits at a timing of transitions of the first beat signal, the pair of digital flip-flop circuits being adapted to sample the second beat signal on respective rising and falling edges of the first beat signal.

Claim 17 (currently amended) A digital frequency detector as claimed in claim 14, wherein the counter means comprises:

a) a first digital edge detector circuit responsive to the multiplexor to generate an enable signal at a timing corresponding to transitions of the third beat signal;

b) a second digital edge detector circuit adapted to generate a reset signal at a timing corresponding to transitions of a sample clock; and

c) a digital counter circuit adapted to count cycles of the enable signal and to generate a pulse count signal indicative of the number of pulses of the enable signal counted between reception of consecutive pulses of the reset signal.

Claim 25 (currently amended) A digital frequency detector as claimed in claim 24, wherein the means for generating a reset signal comprises a $2^M$ frequency divider (where M is a

positive integer) adapted to generate the reset signal by frequency-division of the oscillator output signal.

Claim 28 (currently Amended) A digital frequency detector as claimed in claim 27, wherein the fixed window phase lock indicator further comprises:

a) a digital flip-flop circuit adapted to sample the over-flow signal at a timing of the reset signal; and

b) a logical-NOR gate adapted to assert a value of the lock-indicator signal corresponding to a value of one of the over-flow signal and an output of the digital flip-flop circuit.

Claim 40 (currently amended) A system as claimed in claim 32, wherein the first sample means comprises:

a) a pair of digital latch circuits respectively adapted to sample the oscillator output signal on rising and falling edges of the data signal; and

b) a multiplexor adapted to selectively switch between respective outputs of the pair of digital latch circuits on transitions of the data signal.

Claim 41 (currently amended) A system as claimed in claim 32, wherein the second sample means comprises:

a) a pair of digital latch circuits respectively adapted to sample the quadrature clock signal on rising and falling edges of the data signal; and

b) a multiplexor adapted to selectively switch between respective outputs of the pair of digital latch circuits on transitions of the data signal.

Claim 47 (currently amended) A system as claimed in claim 32, wherein the lock-detecting means comprises:

a) frequency counter means for quantitatively determining a frequency difference between the oscillator output signal and the data signal, and generating a threshold indicator signal indicative of whether the frequency difference is greater or less than a predetermined threshold value; and

b) a state machine adapted to debounce the threshold indicator signal to generate a lock-indicator signal.

Claim 49 (currently amended) A system as claimed in claim 48, wherein the third beat signal is generated by a multiplexor adapted to alternately select respective outputs of each of a first and second digital flip-flop circuit at a timing of transitions of the first beat signal.

Claim 52 (currently amended) A system as claimed in claim 48, wherein the frequency counter means comprises:

a) a first digital edge detector circuit responsive to a fourth sample means to generate an enable signal at a timing corresponding to transitions of the third beat signal;

b) a second digital edge detector circuit adapted to generate a reset signal at a timing corresponding to transitions of a sample clock; and

c) a digital counter circuit adapted to count pulses of the enable signal and to generate a pulse count signal indicative of the number of pulses counted between reception of consecutive pulses of the reset signal.

Claim 58 (currently amended) A system as claimed in claim 35, wherein the lock-detecting means is a fixed window phase lock indicator adapted to generate the lock-indicator signal on a basis of a proportion of time, in relation to a predetermined sample period, for which the second beat signal is at a logical-low level.

Claim 63 (currently amended) A system as claimed in claim 62, wherein the fixed window phase lock indicator further comprises:

a) a digital flip-flop circuit adapted to sample the over-flow signal at a timing of the reset signal; and

b) a logical-NOR gate adapted to assert a value of the lock-indicator signal corresponding to a value of one of the over-flow signal and an output of the digital flip-flop circuit.

Claim 66 (currently amended) A system as claimed in claim 64, wherein the sliding window phase lock indicator comprises:

a) an input digital flip-flop circuit adapted to sample the second beat signal at a timing of a predetermined sample period;

b) an N-bit shift register connected to the input digital flip-flop circuit and adapted to store N consecutive samples of the second beat signal;

c) a first logic gate adapted to assert a high value of a first gate output signal when at least one of the N bits of the shift register, and an output of the input digital flip-flop circuit are at a low value;

d) a second logic gate adapted to assert a high value of a second gate output signal when all N bits of the shift register are at a high value; and

e) an output digital flip-flop circuit adapted to assert a value of the lock-indicator signal based on the first and second gate output signals.

Claim 67 (currently amended) A method of recovering a clock signal from a received data signal, comprising the steps of:

a) sampling the received data signal using a phase detector that generates a phase error signal indicative of a detected phase difference between the data signal and an oscillator output signal, and a digital frequency detector that performs frequency lock on data signal frequencies that fall outside of a pull-in range of the phase detector;

b) selecting an output of the phase detector when a detected frequency difference is small and otherwise selecting the output of the digital frequency detector to generate the recovered clock signal; and

c) using the selected one of the outputs of the phase detector and the digital frequency detector to control an oscillator to generate the recovered clock signal

wherein the digital frequency detector performs the steps of:

i) sampling an in-phase clock at a timing of a data signal to produce a first beat signal;

ii) sampling a quadrature clock signal at a timing of the data signal to produce a second beat signal;

iii) sampling the second beat signal at a timing of the first beat signal to produce two differential outputs.

Claim 70 (currently amended) A method as claimed in claim 67 wherein the two differential outputs determine whether a frequency of the recovered clock signal must be increased, decreased or remain unchanged to match a data signal frequency of the received signal.

Claim 73 (currently amended) A method as claimed in claim 67 wherein operations for recovering the clock signal begin in a reference tracking mode in which the phase detector controls an oscillator to lock to a supplied reference clock, and when a frequency difference between the reference clock and the recovered clock signal is less than a predetermined threshold, the frequency of the recovered clock signal relative to data frequency is monitored.

Claim 74 (currently amended) A method as claimed in claim 73 wherein if a difference in a frequency match is smaller than a predetermined threshold, a transition is made to a data tracking mode in which the digital frequency detector controls a frequency of the recovered

clock signal to reduce the difference in frequency match between a frequency of the recovered clock signal and a frequency of the data signal.

Claim 75 (currently Amended) A method as claimed in claim 74 wherein after the digital frequency detector has controlled a frequency of the recovered clock signal to an extent that a difference between the frequency of the recovered clock signal and the frequency of the data signal is less than the predetermined threshold, control of the recovered clock signal is returned to the phase detector.

Claim 77 (currently amended) A method as claimed in claim 67 wherein clock recovery is performed without a reference clock, comprising the steps of:

a) data frequency acquisition is performed using the digital frequency detector and the frequency of the recovered clock signal is adjusted until the frequency is within a pull-in frequency range of the phase detector; and

b) control is switched to the phase detector to lock the frequency of the recovered clock signal to the frequency of the data signal.

## EXAMINER'S STATEMENTS OF REASONS FOR ALLOWANCE

2. Claims 1-32, 35, 36, 38-68, and 70-78, which have been renumbered claims 1-74, respectively, are allowable over prior art if above rejections are overcome because related references do not disclose a digital frequency detector which includes a first and second sampler

(wherein the second sampler samples a quadrature clock signal) that produce outputs to a third sampler with determines a frequency error signal from the outputs of the first and second sampler.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chan et al. (U. S. Patent No. 6, 411, 665) discloses a digital frequency detector which also samples a quadrature clock signal in order to detect the frequency.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Curtis Odom
October 21, 2004

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